

# A Low Phase Noise Octave-Band Synthesizer Using an X-Band Frequency Reference

Sergey Beltchicov, Andrey Dzisiak and Igor Guletskiy ELVIRA Production Co. Ltd., Russia

An ultra-low phase noise synthesizer with more than an octave tuning capability uses an indirect multiple PLL approach based on an X-Band frequency reference. Measurements of the prototype synthesizer's phase noise performance are made and are believed to be among the best results achieved to date.

ny modern microwave system whether in communications, aerospace or de-Lifense market could be hardly imagined without one of its indispensable components a frequency synthesizer. The key performance criterion for any frequency synthesizer along with requirements for tuning speed, size and resulting cost is the spectral purity of the generated signal which can be evaluated in terms of residual phase noise level and unwanted signals (harmonics, spurious) rejection. The spectral purity of the generated signal will most likely be the prevailing characteristic of a highend frequency synthesizer used for research and reference measurements at the test bench. A study of modern high-end synthesizer architectures<sup>1</sup> reveals several observations:

- A high performance microwave synthesizer will likely use either direct analog synthesis or an indirect synthesis approach using multiple PLLs (with the latter being a more frequent case).
- Indirect synthesis using PLLs will likely use some implementation of frequency conversion in the voltage controlled oscillator (VCO)/YIG-tuned oscillator (YTO) feedback path to suppress excessive phase noise.
- A major hindrance to further improvement of high performance synthesizer phase noise (for both direct analog synthesis and indirect synthesis using PLLs) is deviation from the 20logN rule due to non-ideal multiplication of the 100 MHz oven controlled crystal oscillator (OCXO) references.

**Figure 1** shows the typical phase noise performance of several high-end frequency synthesizers. The blue curve shows the best commercial PLL synthesizer (using a YTO as a tuned oscillator in a frequency offset scheme) at 10 GHz. The red curve shows the best result of ultra-low phase noise OCXO multiplication up to 10 GHz. This will likely be the best obtainable



Fig. 1 Typical synthesizer phase noise performance.



Fig. 2 Phase noise of SLCO reference at 10 GHz.



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result for a direct analog synthesizer using a 100 MHz OCXO as a reference oscillator. The green curve shows the PLL noise floor in a frequency conversion PLL. It is the sum of direct digital synthesizer (DDS) and phase frequency detector (PFD) phase noise at an arbitrarily chosen reference frequency of 100 MHz (with no frequency division in the loop). This green curve also provides a fair representation of good phase noise performance for a small step synthesizer in a direct analog synthesis approach.

From the graphs in Figure 1 it

is clear that if there was some way to increase the quality of the reference frequency used in a frequency conversion PLL (or used as a coarse step synthesizer in the direct analog approach), dramatic improvements could be achieved in phase noise performance up to the limitations imposed by the PLL noise floor (or by the small step synthesizer phase noise in the direct analog approach). The proposed solution is to use an X-Band fixed frequency source for the reference frequency generation instead of multiplying 100 MHz OCXOs.



🔺 Fig. 3 Prototype synthesizer simplified block diagram.



#### DESIGN

For the 10 GHz frequency reference, a sapphire loaded cavity oscillator was used; however, a 10 GHz opto-electronic oscillator (OEO) can be used as well. The 10 GHz frequency reference used in the design does not represent the state-of-the-art for SLCO performance; however, it is sufficient for this design purpose (see *Figure 2*). The 10 GHz low phase noise frequency reference technology is not addressed here, which has been thoroughly investigated by others<sup>2-9</sup> with results being generally better than this report.

The prototype is a triple offset loop synthesizer (see Figure 3). The first offset loop is used to phase-lock a Hittite VCO to a 10.2 GHz SLCO to achieve 200 MHz of synthesized tuning around 10 GHz while preserving the low phase noise of the sapphire reference. We use a broadband 3.5 Gsps DDS for better spurious in the tuning range with additional suppression provided by varying the clock frequency and by using the PLL as a spurious filter. The spurious signals are further suppressed to an acceptable level of <-80 dBc by dividing the 200 MHz tuning range of the 9.95 to 10.15 GHz first loop synthesizer into the frequency range of 4975 to 5075 MHz, which is then used as a tunable reference for the second offset loop.

The second loop increases the 100 MHz tuning range of the first loop synthesizer by a factor of 11. This is



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accomplished by changing the comparison frequency in coarse steps and using both sidebands of the loop frequency conversion. We use two low noise VCOs, one for each sideband, to optimize the resulting phase noise profile of the second loop synthesizer. Also, doublers are used in the loops to additionally lower the phase noise of the locked VCOs in cases where the inherent PFD noise floor becomes high (see Table 1). The fixed reference signals of 50, 200, 300, 800 and 1000 MHz are all derived from an ultra-low noise 100 MHz OCXO which is also used to phase-lock the SLCO for long term frequency stability.

The switched second loop synthesizer provides a 1100 MHz tuning range with the phase noise performance shown in *Figure 4*. The loop bandwidth is kept around 3 MHz for





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	TABLE I								
	FREQUENCY AND PHASE NOISE AT SEVERAL LOCATIONS								
	VCO 1 after Division (MHz)	IF/REF Frequency (MHz)	Phase Noise VCO 1:N/REF/ PFD (dBc/Hz)	VCO 2 and VCO 3 (MHz)	Effective Phase Noise VCO 2/ VCO 3 (dBc/Hz)				
	4975 to 5075	-500/1000	-153/-160/-149	4475 to 4575	-147				
	4975 to 5075	-400/800	-153/-162/-150	4575 to 4675	-148				
	4975 to 5075	-300/300	-153/-164/-148	4675 to 4775	-147				
	4975 to 5075	-200/200	-153/-168/-150	4775 to 4875	-148				
	4975 to 5075	-100/100	-153/-174/-153	4875 to 4975	-150				
	5025 to 5075	-50/50	-153/-164/-156	4975 to 5025	-151				
	4975 to 5025	+50/50	-153/-164/-156	5025 to 5075	-151				
	4975 to 5075	+100/100	-153/-174/-153	5075 to 5175	-150				
	4975 to 5075	+200/200	-153/-168/-150	5175 to 5275	-148				
	4975 to 5075	+300/300	-153/-164/-148	5275 to 5375	-147				
	4975 to 5075	+400/800	-153/-164/-150	5375 to 5475	-148				

-153/-164/-149

5475 to 5575

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both VCOs. This second loop synthesizer maintains spurious content below -80 dBc across the entire tuning range.

To achieve an octave tuning range in the microwave region, the third offset loop uses the second loop synthesizer as a tunable offset reference to phase lock a 9 to 18 GHz YTO. Shown in Figure 3, dividers are used in the loop to pull the YTO into the narrower range of the second loop synthesizer. The division ratio is kept as low as possible, with N=3 being the maximum division value. This is achieved by switching the IF (comparison frequency at the PFD) and using double conversion (double offset) in the loop (see **Table 2**).

#### **MEASUREMENTS**

Phase noise of the synthesizer is measured by mixing output signals from two prototype synthesizers in a Marki M8-0326MS double balance mixer and applying the resulting IF (100 MHz) to the Agilent E5052A signal source analyzer. Assuming that the phase noise of both prototype synthesizers is essentially equal, we apply a 3 dB correction to the measured results. The measured phase noise performance for output frequencies of 10 and 18 GHz (see Figure 5) is at least 10 dB lower than that of any commercially available general purpose synthesizer. Spurious performance of this octave-band synthesizer is better than -70 dBc. If this synthesized core is used to provide lower frequency coverage by means of octave frequen-

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TABLE II           FREQUENCY AND PHASE NOISE AS A FUNCTION OF THE FREQUENCY DIVIDER RATIO								
VCO 2 & VCO 3 (MHz)	YTO Output Frequency (MHz)	N	Phase Noise 2nd Loop Synth/Divider/PFD/REF + 20logN (worst case) (dBc/Hz)	IF/PFD Comparison Frequency (MHz)				
4475 to 5575	9050 to 11250	2	-147/-153/-156/-164 = -140	50/50				
4575 to 5575	11250 to 13250	2	-147/-153/-156/-164/-154 = -139	1050/50				
5325 to 5525	13250 to 13650	2	-147/-153/-148/-164/-154 = -137	1300/300				
4500 to 5575	13650 to 16875	3	-147/-153/-156/-164 = -136	50/50				
4575 to 5575	16875 to 19875	3	-147/-153/-156/-164/-156=-136	1050/50				

cy division and careful subsequent filtering, its phase noise and spurious performance will further improve following the 20logN rule.

### CONCLUSION

It has been demonstrated that the use of an X-Band fixed frequency reference can overcome the phase noise performance limitations of traditional multiplicative schemes. The proposed solution is just the first implementation (and possibly not the best) of an SLCO-based synthesizer; however, it offers a significant improvement (>10 dB) over results previously advertised as best in the industry for a commercially available general purpose synthesizer. Further performance improvements are planned: reducing the spurious performance to <-90 dBc, providing better phase noise performance at offset frequencies <10 kHz by adding some fast circuit switching



Fig. 5 Prototype synthesizer SSB phase noise.

(FCS) to the reference SLCO, and offering a direct analog core built around the SLCO to meet requirements for extremely low phase noise and high switching speeds in a microwave synthesizer. ■

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Sergey A. Beltchicov received his M.Sc. degree from Lomonosov Moscow State University in 2001 and his PhD degree from Moscow Power Engineering Institute in 2003. He is vice president of engineering and co-owner of ELVIRA Co. Ltd., Zheleznodorozhny, Russia. His main scientific interests are associated with ultra-low noise signal generation and synthesis at microwave frequencies.

**Andrey B. Dzisiak** received the M.Sc. from his Belarussian State University

of Informatics and Radiotechniques, Minsk, Belarus, in 1996, and PhD degree from the Moscow Technical University of Communications and Informatics, Moscow, Russia, in 2008. His PhD thesis involved experimental and theoretical studies of phase noise measuring systems for microwave signals. He has been working for ELVIRA Co. Ltd. since 2007. Since 2009 he has been the chief of microwave business unit in the company. His recent interests include precision phase noise metrology, low noise frequency synthesis, design and manufacture of sophisticated measuring systems for the frequencies up to 178 GHz and their metrology maintenance.

**Igor N. Guletskiy** received his M.Sc degree from Moscow Power Engineering Institute (MPEI, Moscow, Russia). He has been working for more than 15 years in R&D department of ELVIRA Co. Ltd., Zheleznodorozhny, Russia, holding various positions from engineer to the chief of the synthesis group. His primary areas of expertise are RF and microwave frequency synthesizers, low-noise und ultra-low noise microwave oscillators and crystal-controlled oscillators.

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