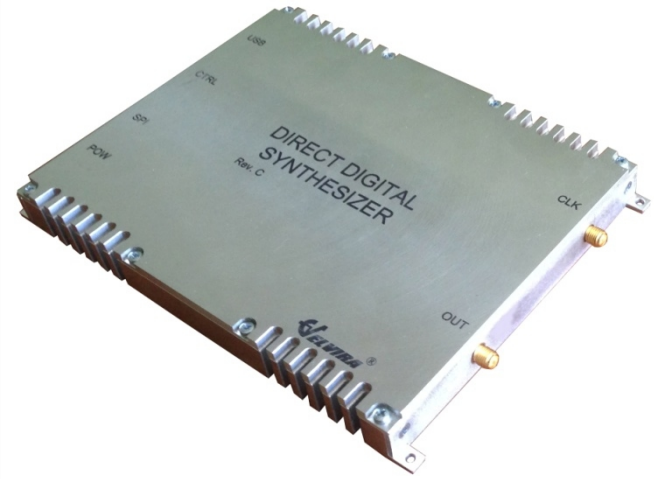
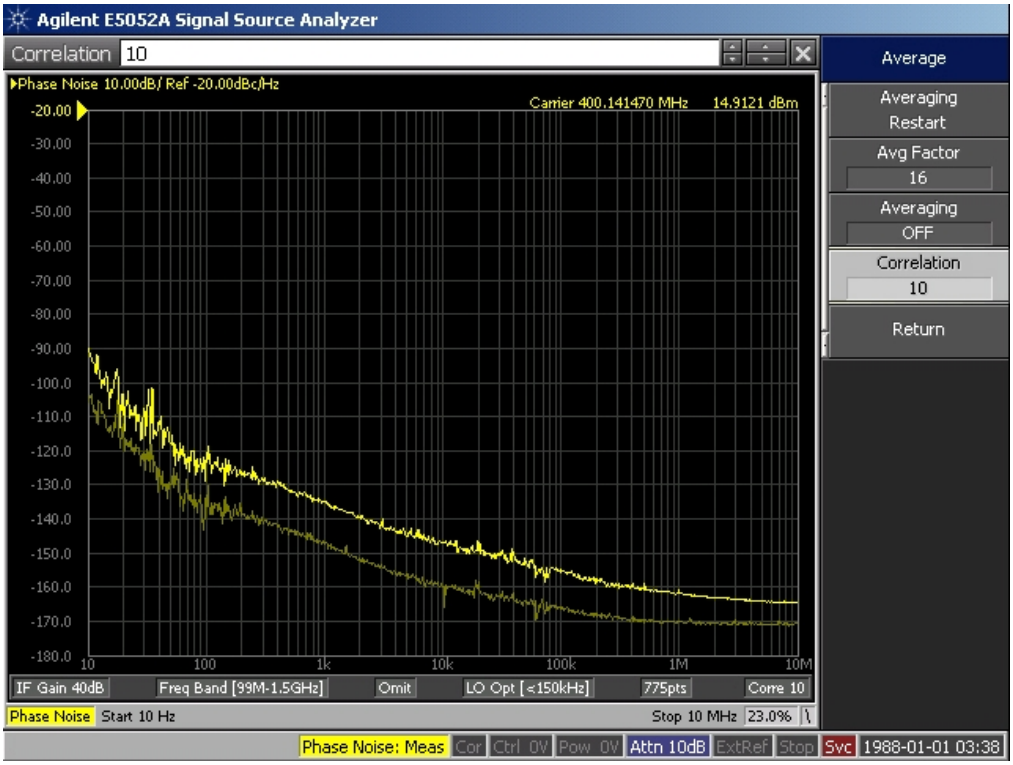


ELV-DDS is a direct digital synthesizer module built on a combination of a modern high-speed 14-bit DAC and Kintex-7 FPGA. This synthesizer requires a 3.2 GHz clock frequency and features a specified output frequency range from DC to 600 MHz (usable up to 1.5 GHz with a degraded spur and output power performance). If the clock is supplied from a low phase noise source (e.g. ELV-OCXO 100 plus KFSM) the synthesizer will provide an output signal with phase noise as low as -146 dBc/Hz (at 10 kHz offset from a 500 MHz carrier). The main advantage of the ELV-DDS which places it truly apart from its commercially available counterparts (e.g. AD9914) is its unique spur performance. In the frequency range from DC to 600 MHz the ELV-DDS generates a clean output spectrum with no spurs >-90 dBc due to a sophisticated spur cancellation algorithm (activated by default, can be disabled at user's discretion). Even at frequencies around F_{CLK}/N which are traditionally contaminated with high order spurs in commercial DDS chips, the ELV-DDS features no spurs exceeding -90 dBc. The module is equipped with USB, SPI and parallel control interfaces. The switching speed is around 15 ns between any two frequencies if the unit is controlled via the parallel interface. Despite such tuning agility a continuous phase is preserved during any frequency transitions. The unit is capable of any custom modulation with an entire 600 MHz bandwidth and there is enough room for user specific modulation schemes accessible in its FPGA. The output power is >+10 dBm across the specified frequency range. The ELV-DDS comes in a robust aluminum milled case and operates over the frequency range of 0…+50°C. The module draws 1200 mA from a 9 V power supply and needs to be mounted on a conductive heat sink.

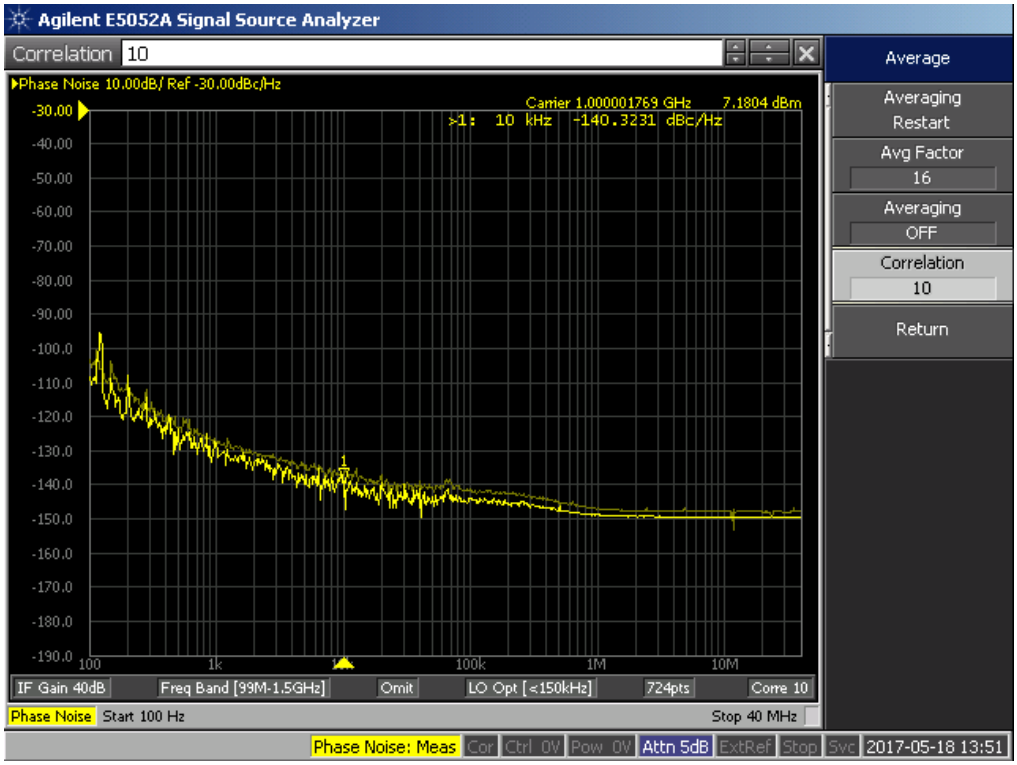
Parameter Description	Parameter Value	
Frequency Range	DC – 600 MHz (usable across the entire 1st Nyquist zone)	
Frequency Step	0.000001 Hz	
Clock Frequency	3200 MHz	
Output Power	> +10 dBm	
SSB Phase Noise (F_{CLK} is generated from ELV-OCXO 100 plus KFSM)	100 MHz carrier	1 GHz carrier
1 Hz offset	-70 dBc/Hz	-50 dBc/Hz
10 Hz offset	-105 dBc/Hz	-85 dBc/Hz
100 Hz offset	-135 dBc/Hz	-105 dBc/Hz
1 kHz offset	-150 dBc/Hz	-130 dBc/Hz
10 kHz offset	-160 dBc/Hz	-140 dBc/Hz
100 kHz offset	-165 dBc/Hz	-145 dBc/Hz
1 MHz offset	-170 dBc/Hz	-150 dBc/Hz
Spurs	<-90 dBc	
Harmonics	<-30 dBc	
Switching Speed	15 ns	
Real-time Update Rate (via the parallel interface)	>400 MB/s (48 bit tuning word)	
Power Supply Voltage (Volts)	+9 V	
Current Consumption (mA)	1200 mA	
Operating Temperature Range	0…+50°C	

Clock In / Output Connectors	**SMA (f)**
Control Connectors	**USB mini B (receptacle), SPI (14 pin, 2.0 mm pitch, Molex 878331421), parallel (50 pin, 1.27 mm pitch, TE Connectivity 5-104069-2)**
Power Supply Connector	**TE Connectivity 2-1445098-4**
Case and Dimensions	**Milled Aluminum Case 165 mm x 130 mm x 18 mm**

ELV-DDS Phase Noise Plots at Various Frequencies
100 MHz (memory trace) and 400 MHz (data trace)

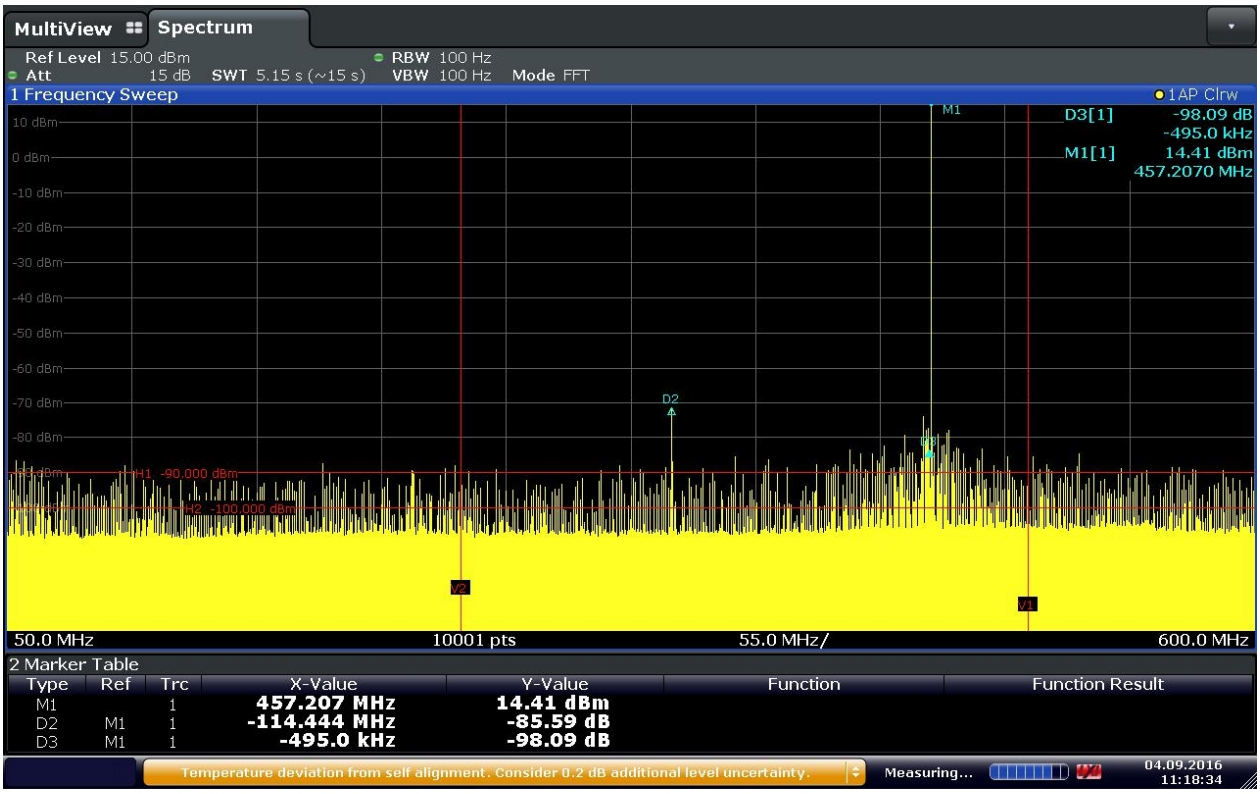


1000 MHz (data trace) and 1500 MHz (memory trace)



Examples of Spur Cancellation Algorithm Implementation

Spurs before Cancellation Algorithm Activation ($F_{OUT} = F_{CLK}/7+dF$, Wide Span)



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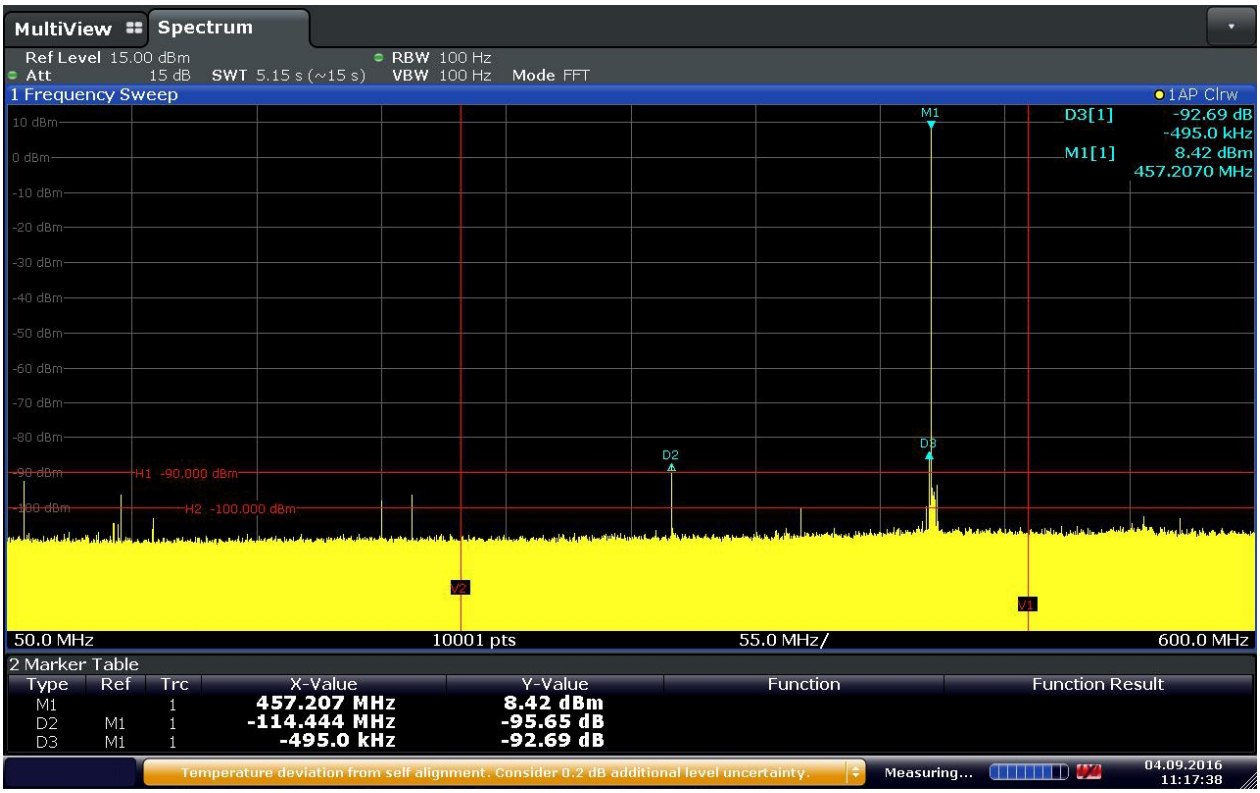
Spurs with Cancellation Algorithm Activated ($F_{OUT} = F_{CLK}/7+dF$, Wide Span)



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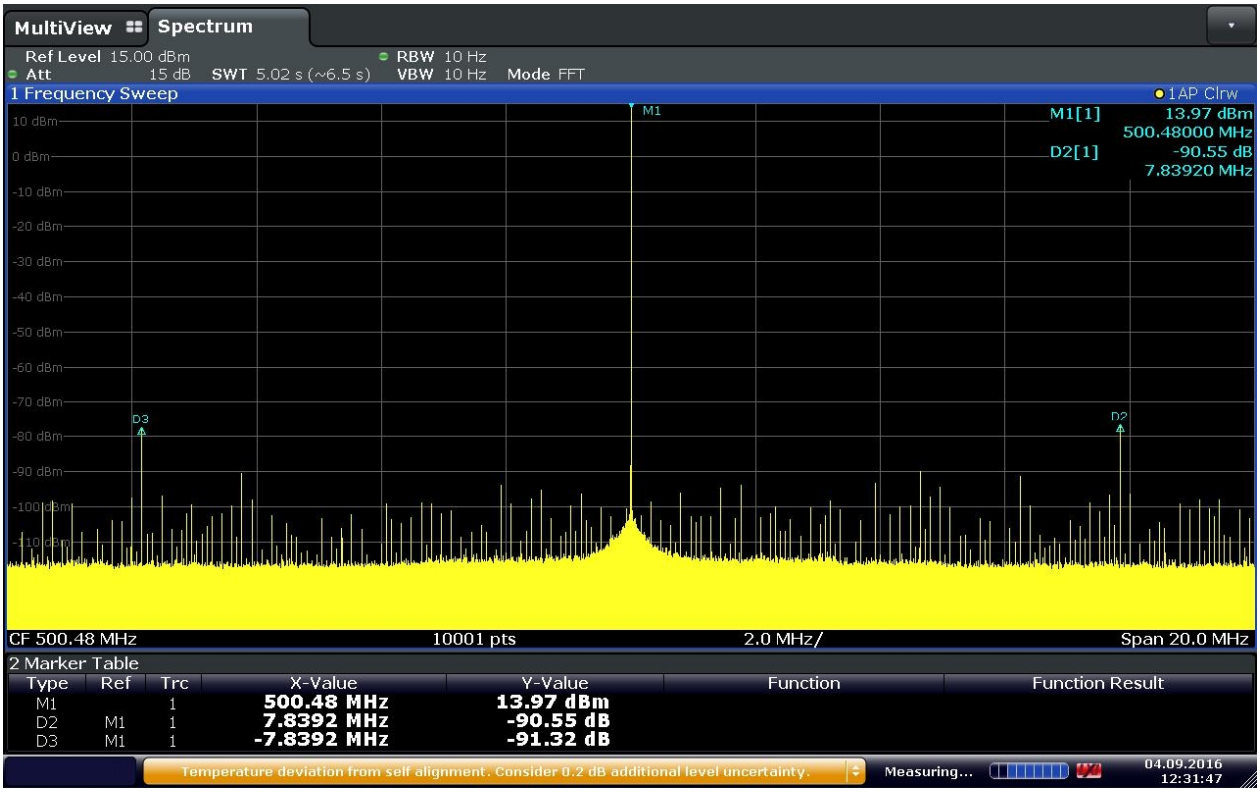
Spurs before Cancellation Algorithm Activation (F_{OUT} = 500.48 MHz, 20 MHz Span)



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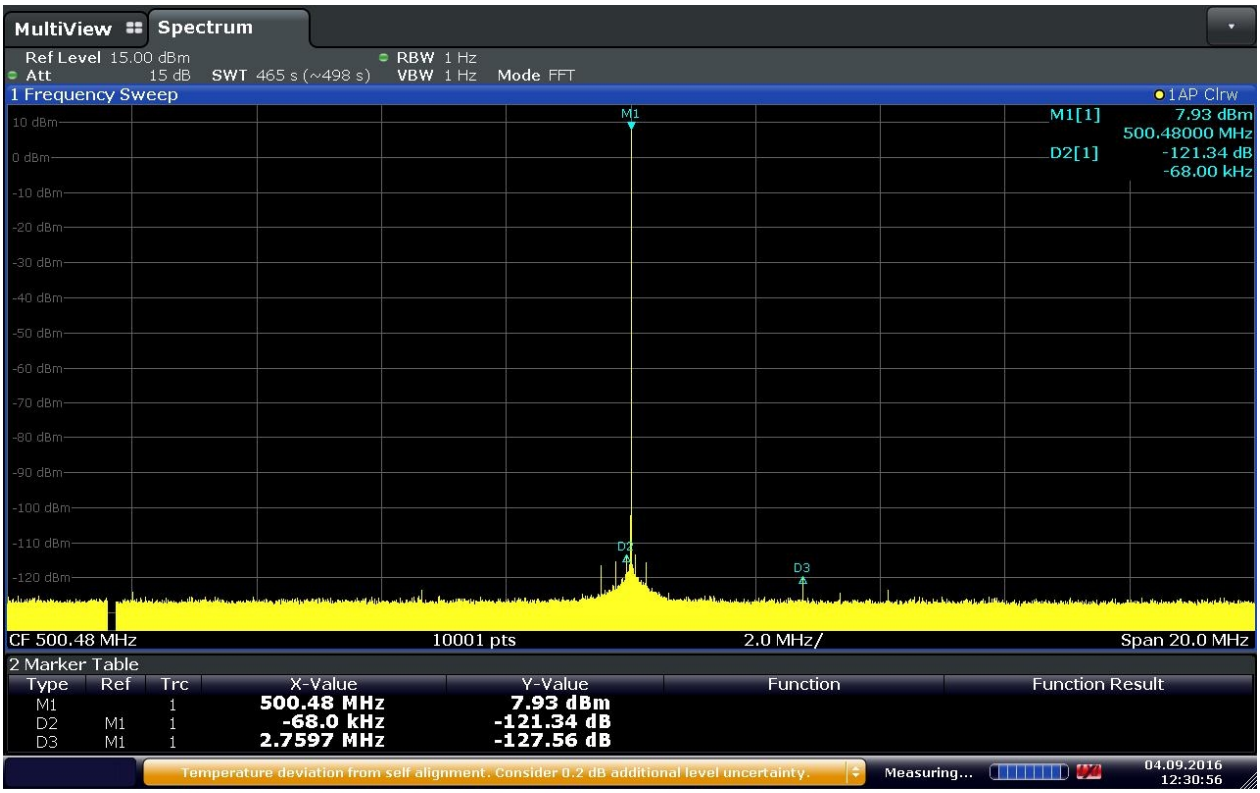
Spurs with Cancellation Algorithm Activated (F_{OUT} = 500.48 MHz, 20 MHz Span)



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